Single-Pole Double-Throw Switch and Low-Noise Amplifier for a 2.5 GHz Full-Duplex Front-End

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***Abstract*—Colorado School of Mines is home to an engineering course entitled: Active Radio Frequency and Microwave Devices (EENG 529). As a semester final project a team of three students were tasked with a real world engineering problem where they were expected to design and fabricated active devices that could be used in a full-duplex front-end; namely, a single-pull double-throw switch consisting of pin diodes, and a low-noise amplifier. The system is designed to operate within the WLAN with a specified operating frequency of 2.5 GHz. The students used Keysight ADS a commercial computer aided design tool with built in full wave simulation technology in conjunction with several core concepts to active microwave devices to deliver strong simulated and measured results.**

I. Summary of Design Parameters

THE requirements of note for the components are as follows:

SPDT Metric	Target	LNA Metric	Target
Return Loss	> 14 dB	Return Loss	> 10 dB
Insertion Loss	< 1.5 dB	Gain	< 10 dB
Isolation	≥ 20 dB	Noise Figure	< 3 dB

Design criteria.

60 mil Rogers 3003 substrate was selected for it's low dielectric losses, it's permissibility for milling in Labriola, and it's compliance with existing connectors in the lab.

II. Single Pull Double Throw Switch

A. Design Motivation and Approach

A high isolation SPDT switch topology was selected from recommendations in the Skyworks High Power Switch Design Guide as shown in Fig. 1. The C_{block} capacitors at the RF inlet and outlets combine with the RF choke inductors to form matching L-sections, reducing return loss and improving isolation.

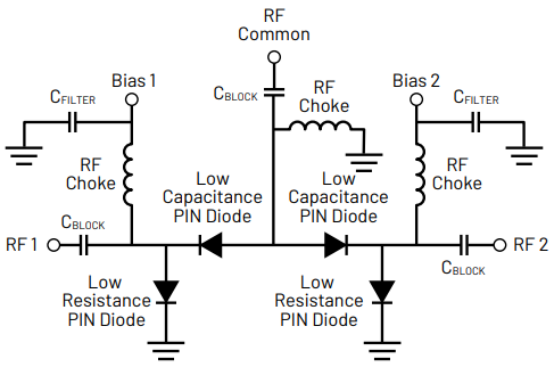

Fig. 1: SPDT Switch Topology

B. Relevant Theory and Design Equations

The target values for the common RF choke (L-feed) and the C_{block} (C_{feed} at the inlet and C_{load} at the outlet) capacitors were estimated by analytically solving for impedance matching in the 'ON' state resulting in the solution surface shown in Fig. 2. This revealed that selecting $L_{feed} \sim 20$nH should enable a match across a reasonable range of C_{block} capacitances.

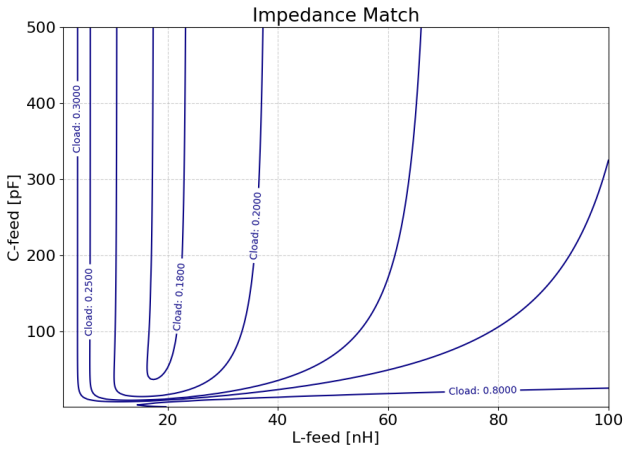

Fig. 2: Impedance matching the SPDT 'ON' state.

Following this initial parameterization, the phase delay through each lumped element was measured and each signal path was mapped according to Fig. 3. A system of linear equations was solved to provide initial microstrip lengths to ensure the target path appeared as an RF short and all other paths appeared as an RF open circuit using $\frac{\lambda}{4}$ relations.

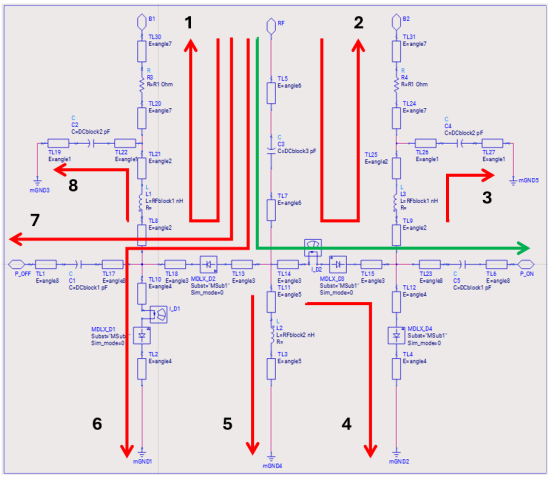

Fig. 3: Signal path mapping for $\frac{\lambda}{4}$ analysis.

C. Simulation Results

The system performance following optimization and converting lumped components to their non-ideal models is shown in Fig. 4 with the layout indicated in Fig. 5. Fabrication and measurement of the device was attempted but ultimately failed due to hardware limitations with the available milling machine. The simulated result exceeds all target specifications over approx. 100 MHz bandwidth.

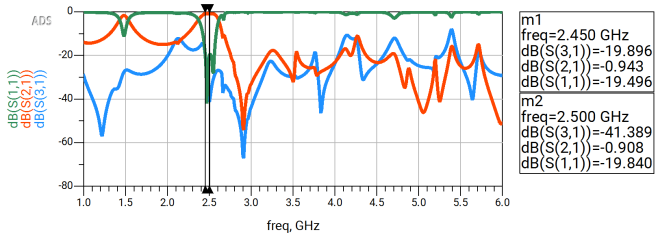

Fig. 4: Performance of SPDT switch.

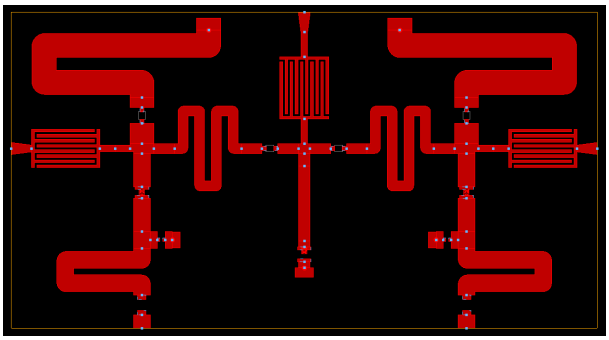

Fig. 5: SPDT switch layout.

III. Low Noise Amplifier

The process of the Low noise amplifier design consisted of several stages: Bias network, Matching, Layout and simulation, and optimizaiton.

A. Bias Network

The to build the biasing network, we had to first identify the needed biasing. First, we placed the Infineon model of the transistor into ADS IV Curves DesignGuide to determine the necessary bias point. In order to pick a point in Class A operation, we chose 2V and 300μA. To properly supply this, we created a circuit to supply the proper bias conditions. Solving the circuit finds the resistors to be 4.3k and 22 ohms respectively. The final step in the biasing network was to determine the capacitance of the DC Block and the inductance of the DC Feed, which we determined to be 32pF and 32nF respectively.

B. Matching Network

Open shunt stub matching is used to present the amplifier with the impedance required for minimum noise figure. Using the ADS BJT Matching DesignGuide and Smith chart tools, the load and source are matched with transmission line networks.

C. Layout and simulation

Now that our network is made, we now place discontinuities to create the layout and perform simulations. All specifications were met when balancing the design criteria with optimization the length of the transmission line matching networks.

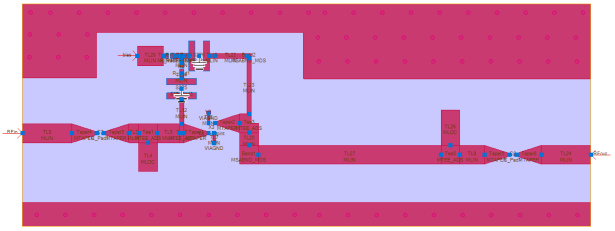

Fig. 6: LNA Layout.

Iteration of design illustrated that if noise figure was targeted as the primary goal for optimization higher forward transmission gain, lower noise figure, and still better than specified matching is achievable.

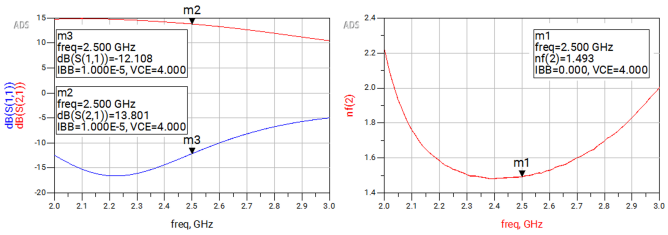

Fig. 7: Results for Optimization with Noise Figure Priority.

D. Manufacturing

The manufacturing of the LNA was not trivial. Once the Gerber files were generated in ADS, We converted it to a SVG file. Using both gerber and SVG in the Bantam Tools Software, we were able to mill out the LNA. Once milled, we soldered the vias and parts.

E. Simulated Versus Measured Results

The LNA was manufactured and measured using a vector network analyzer and spectrum analyzer. The first measurement involved attaching port 1 of a vector network analyzer to the LNA and attaching port 2 in series with 40 dB of attenuation to the otuput of the LNA. Then biasing the transistor.

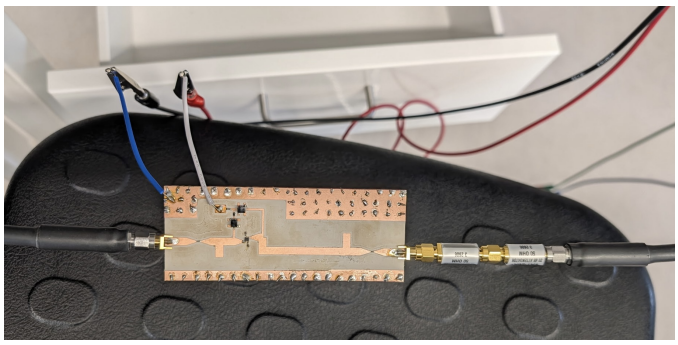

Fig. 8: Measurement Setup for LNA S Parameters.

The next measurement involved using a vector network analyzer as a signal source (sweeping power form -15 to 2 dBm) for the LNA and measuring the output with no attenuation using a spectrum analyzer. To confirm the LNA was providing a good signal source we plugged it directly into

the spectrum analyzer and confirmed the input power matched the output power.

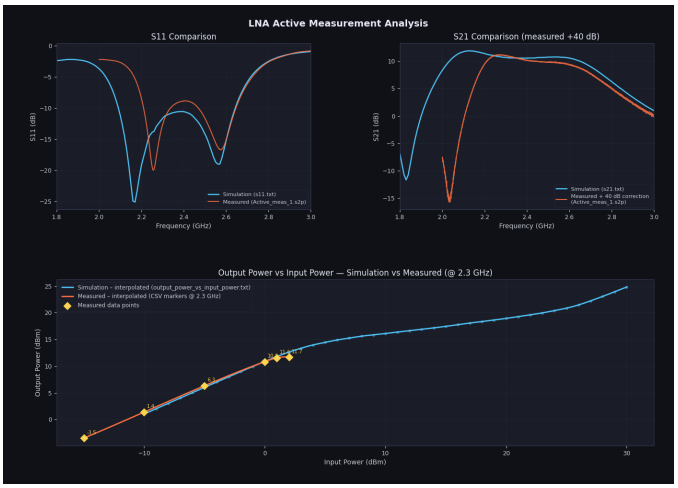

Fig. 9: Measured Vs Simulated Results.

The differences observed in the s parameter behavior can be explained by the dielectric pedestal effect from cutting too deep into the substrate because of achievable tolerance of the circuit mill available. This means the effective dielectric constant substrate is altered causing a frequency shift. The VNA was not a stable RF source past 2 dBm of input power but there is strong correlation in the linear region of operation.

IV. Mixing Demonstration

For system level characterization the team participated in a demonstration where we emulated an RF reception. A block diagram of the setup is shown in the figure below:

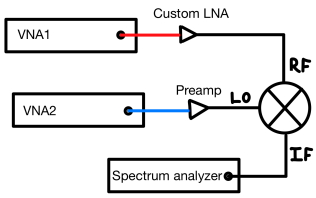

Fig. 10: System Level Characterization Block Diagram

VNA1 in the figure figure above is supposed to emulate an antenna receiving some signal, so we use a low power input, this is then amplified with the low noise amplifier and fed into the RF port of a mixer. The VNA2 provides a local oscillator tone 100 MHz away from the expected RF input so that the mixing product forms an intermediate frequency at 100 MHz allowing easy analog digital sampling and down stream demodulation. We sampled the intermediate frequency and harmonics using a spectrum analyzer, we noticed as the input power to the LNA increased we got more and more power in the harmonics which is consistent with the linearity analysis presented earlier.

V. Conclusion

The designed low-noise amplifier (LNA) successfully met the specified performance requirements at the intended operating

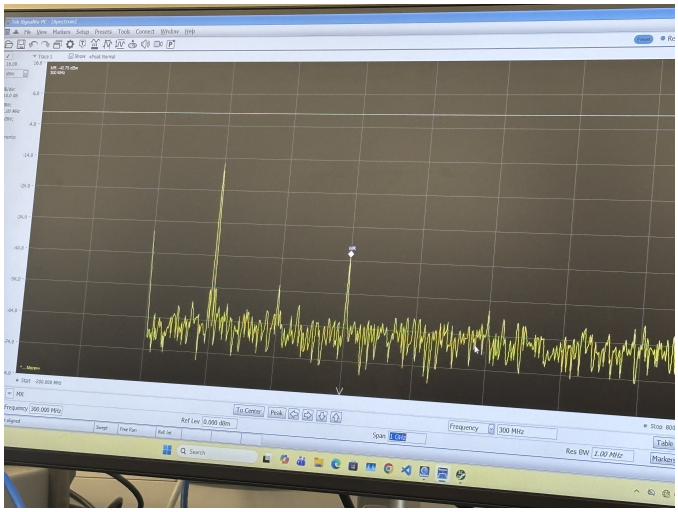

Fig. 11: Spectrum Analyzer IF Output.

frequency. Measured results showed strong agreement with simulation, with only a minor frequency shift observed, likely attributable to fabrication tolerances and component parasitics. Although only the LNA was fabricated due to a circuit mill failure, the design and simulation results for the single-pole double-throw (SPDT) switch indicate a high likelihood of successful operation. An additional iteration of the LNA was explored at the schematic level, prioritizing noise figure during optimization. This iteration demonstrated improved noise performance and bandwidth, suggesting a viable path for further enhancement in future work. The team also participated in a system-level mixing demonstration, in which multiple network analyzers were used to generate the local oscillator and RF input signals. The RF signal, amplified by the LNA, was successfully mixed to produce an intermediate frequency suitable for sampling by an analog-to-digital converter. Notably, this implementation resulted in a fully functional device, distinguishing the team as the only group to achieve successful operation under the given constraints. Overall, the results validate the design methodology and highlight the robustness of the implemented LNA, while also identifying opportunities for continued refinement and system integration.

VI. In Memoriam: Dr. Art Morris

We wish to dedicate this report and the culmination of our work to the memory of Dr. Art Morris, whose influence is woven into every page of this project.We are profoundly grateful for the countless hours he poured into our education and for the unwavering dedication he showed to his students.Art did not just teach us the mechanics of high-frequency technology; he taught us the importance of precision, the value of hard work, and the resilience required to excel in the field of engineering.

His legacy lives on in the many engineers he helped shape. Our deepest condolences go out to the Morris family.

Rest in Peace, Dr. Art Morris.